a planar bare die electronic device having a top, a bottom, sides, and a plurality of contacts, the device being disposed in the recess; and

a planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device.

In the Drawings:

A corrected drawing that respond to the objection in paragraph 2 of the office action is submitted herewith.

Remarks

Claims 1-2, 4-22, 32, 34-36 are currently active in the application.

Claims 1, 9, 14, 16, 21, 22, and 32 have been amended to clarify that the electronic device package includes a silicon wafer that includes a recess for inserting an electronic device. The examiner's attention is drawn to the present application, page 3, lines 1-10. The examiner's attention is also drawn to page 4, lines 13 to 20, where a method of producing the device is described that clearly identifies a silicon wafer as the basis for this packaging structure.

Drawings

The drawings have been objected to as failing to comply with 37 C.F.R. 1.84(p)(5) because they do not include the following reference sign mentioned in the description: page 7, line 6 of the specification refers to a planarizing dielectric material "550". In Fig. 5, the reference number "550" has been added to indicate the planarizing dielectric material. A Letter to the Master Draftsman accompanies this amendment with the correction to the drawing.

The drawings were also objected to as failing to comply with 37 C.F.R. 1.84(p)(4) because reference character "520" on page 7, line 3 of the specification has been used to designate both bare die and device. On page 7, line 1, reference number "520" is introduced as "a bare die planar electronic device 520". The following changes to the specification were made in the response to the previous office action, for consistency: at page 7, line 3, the words "bare die" have been replaced with --device--; at page 7, line 5 the words "bare die" have been replaced with --device--; and on page 7, line 8, the words "bare die" have been replaced with the words "device". With these changes to the specification, the drawings comply with with 37 C.F.R. 1.84(p)(4).

Claim Rejections --- 35 U.S.C. §102(e)

Claims 1-2, 5-22, 32, and 34-36 stand rejected under 35 U.S.C. §102(e) as anticipated by Wyland, U.S. Patent no. 5,986,885.

Claim 1, as amended, now requires,

"1. An electronic component comprising:

an electronic device package including a silicon wafer having a recess, the recess including a conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region."

Wyland teaches a bare die 30, coupled to a die attach paddle 25, which is typically made of thermally conductive material such as copper (see Wyland

at col. 1, lines 30-40 and figure 1). The die attach paddle 25 is further coupled to a thermally conductive metal sponge 40 (see Wyland at col. 5, lines 49-55). An encapsulant 45 is then applied over the entire assembly (see Wyland at col. 6, lines 5-10). Accordingly, fig.1 in Wyland does not disclose the use of a silicon wafer as a layer on which to package an electronic component, nor does it disclose such a wafer having a recess. In fact, a silicon wafer acts as a relatively poor heat conductor and thus would be ineffective at achieving the goal of Wyland's invention, which is providing an internal heat sink for the semiconductor die (see Wyland, Title and Abstract). Since Wyland does not teach a required limitation of claim 1, Wyland cannot anticipate the embodiment of claim 1 of the present application.

Claims 2 and 4-13 which depend from claim 1 and add further limitations are patentable over Wyland for at least the same reasons as for claim 1.

Independent claims 14, 16, 21 and 32, as amended, each require "a package including a silicon wafer with a recess." For the same reasons cited above for claim 1, Wyland does not teach or suggest this limitation. Therefore, Wyland does not anticipate any of claims 14, 16, 21 or 32. Claims 15, 17-20, 22 and 34-36, which each depend from one of 14, 16, 21 or 32, and add further limitations are patentable over Wyland for at least the same reasons as for claims 14, 16, 21 and 32, respectively.

Thus, claims 1-2, 5-22, 32, and 34-36 are deemed patentable under 35 U.S.C. §102(e) over Wyland.

Claims 1, 14, 16, 21, and 32 stand rejected under 35 U.S.C. §102(e) as anticipated by Suzuki et al, U.S. Patent no. 5,977,633.

Suzuki discloses a package that includes a *metal base substrate* having a recess (see Suzuki at fig. 1, and col. 4, lines 18-34), as opposed to a *silicon* wafer having a recess as required by claim 1, as amended. A *silicon* wafer having a recess is neither taught nor suggested by Suzuki. Accordingly, claim 1 is not anticipated under 35 U.S.C. §102(e) by Suzuki. Claims 14, 16, 21, and 32, as amended, require a similar limitation and are deemed patentable over Suzuki for the same reason.

Claim Rejections --- 35 U.S.C. §102(b)

Claims 1, 14, 16, 21, and 32 stand rejected under 35 U.S.C. §102(b) as anticipated by Andros et al. or Corisis or Hernandez et al. or Hebert, U.S. Patent nos. 5,633,533; 5,907,769; 5,095,402; and, 4,649,415, respectively.

As stated above each of claims 1, 14, 16, 21, and 32, as amended, requires an electronic device package including a silicon wafer having a recess.

Andros discloses a package that includes a *thermally conductive* support member 31 having an indentation 33 (see Andros at col. 4, lines 26-28). The support member 31 is preferably a *metal* such as copper (see Andros at col. 4, lines 30-32), and, thus, is not "a silicon wafer having a recess" as required by claims 1, 14, 16, 21, and 32. Since Andros does not teach each element of claims 1, 14, 16, 21, or 32, respectively, claims 1, 14, 16, 21, and 32, respectively, are not anticipated under 35 U.S.C. §102(b) by Andros.

Further, Corisis discloses a semiconductor assembly that includes a semiconductor device 100 that is supported by a lead frame 10 (see Corisis at fig. 1 and accompanying text). The semiconductor device is encapsulated in an epoxy plastic material to form a package 200 (see Corisis at col. 4, lines 41-47). Hence, the semiconductor device 100 is not disposed in a recess of a silicon wafer, as required by each of claims 1, 14, 16, 21, and 32, respectively. Since Corisis does not teach every element of claims 1, 14, 16, 21, and 32, respectively, claims 1, 14, 16, 21, and 32, respectively, are not anticipated under 35 U.S.C. §102(b) by Corisis.

Further, Hernandez discloses a chip 38 that is supported by a lead frame 10 that is encapsulated in a molded package 44 (see Hernandez at col. 4, lines 32-33). Hence, the semiconductor device 100 is not disposed in a recess of a silicon wafer, as required by claims 1, 14, 16, 21, and 32, respectively. Since Hernandez does not teach every element of claims 1, 14, 16, 21, and 32, respectively, claims 1, 14, 16, 21, and 32, respectively, are not anticipated under 35 U.S.C. §102(b) by Hernandez.

Further, Hebert discloses a die 30 that is housed in a polymeric thermoplastic material, such as polyethersulfone, polyethyerimide, or polyphenylene sulfide. (see Hebert at col. 3, lines 16-24. Hence, the die 30 is not disposed in a recess of a silicon wafer, as required by claims 1, 14, 16, 21, and 32, respectively. Since Hebert does not teach every element of claim 1, 14, 16, 21, and 32, respectively, claims 1, 14, 16, 21, and 32, respectively, are not anticipated under 35 U.S.C. §102(b) by Hebert.

Claim Rejections --- 35 U.S.C. §103(a)

Claim 4 stands rejected under 35 U.S.C. §103(a) over Wyland or Suzuki or Andros et al. or Corisis or Hernandez et al. or Hebert in view of Oji et al. or Yoshida, et. al, Japanese Patent nos. 58197857 and 59145537, respectively. As stated above, neither Wyland nor Suzuki nor Andros et al. nor Corisis nor Hernandez et al. nor Hebert teach or suggest a *silicon* wafer having a recess as required by claim 4. Neither Oji or Yoshida teach such a limitation. Since none of these references teach this required limitation of claim 4, the embodiment of claim 4 is deemed nonobvious over any combination of these references.

For the reasons set forth above, it is submitted that all pending claims are now in condition for allowance. Reconsideration of the amended claims and a notice of allowance are therefore requested. If any additional fees are required for the timely consideration of this application, please charge deposit account number 19-4972. The Examiner is requested to telephone the undersigned if any matters remain outstanding so that they may be resolved expeditiously.

Respectfully submitted,

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V rsi n with Markings t Show Changes Made

1. (amended) An electronic component comprising:

an ~~silicon~~ electronic device package including a silicon wafer having a recess, the recess including a conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region.

9. (twice amended) An electronic component according to claim 1, wherein:

the device is a vertical device and the bottom of the device is coupled to ~~the package in~~ the recess.

14. (twice amended) An electronic component comprising:

an electronic component ~~package~~ including a silicon wafer having a recess, the recess including a first ~~deposition processed~~ conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the first conductive region and the top terminal is electrically coupled to a second ~~deposition processed~~ conductive region, and wherein at least a portion of the first and second conductive regions are essentially planar.

16. (amended) An electronic component comprising:

an electronic device package including a silicon wafer having a recess~~a silicon package having a recess~~, the recess including a conductive region; and

an electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal located in a region other than the top of the device, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region.

21. (amended) An electronic component comprising:

an electronic device having a first terminal and a second terminal, wherein a first dimension is defined therebetween;

an electronic device package ~~a silicon package~~ having a first surface ~~and a second surface~~, the ~~silicon~~ package including a silicon wafer having a recess on the first surface that has a depth that is substantially equal to the first dimension, the ~~silicon~~ package further having a layer of metal applied to the recess and ~~a~~ to a portion of the first surface, wherein the electronic device resides within the recess and the second terminal is coupled to the layer of metal; and

a layer of insulation coupling the electronic device to the silicon ~~package~~wafer.

22. (amended) An electronic component according to claim 21, further comprising:

a first contact coupled to the first terminal; and

a second contact coupled to the metal residing on the first surface of the ~~silicon~~ package.

32. (amended) An electronic component comprising:

a non-molded electronic component package having a package top and ~~a recess~~a silicon wafer including a recess;

a planar bare die electronic device having a top, a bottom, sides, and a plurality of contacts, the device being disposed in the recess; and

a planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device.